

M.2 Primer



Understanding and Integrating M.2 Modules...

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1 Document Revision History

<i>Revision</i>	<i>Date</i>	<i>Description</i>
PA1	2019-05-06	First version.

2 Introduction

This document is a description of the M.2 interface and how it is used to create a very flexible system architecture when it comes to adding a Wi-Fi/BT interface in an embedded system. Specifically the solution provided by Embedded Artists is addressed, including an integration guide and information about regulatory certification.

2.1 What is M.2?

M.2 is a standard for internally mounted expansion cards. It is commonly found in ultrabooks, tablets, laptops and PC mother boards. It is also finding its way into more and more embedded systems designs.

The M.2 standard was formerly known as Next Generation Form Factor (NGFF) and has evolved from the mSATA and PCIe mini card standards.

Several different high-speed interface bus standards are supported, like PCIe, Serial ATA, USB and SDIO. M.2 modules can have several different functions implemented, including, but not limited to:

- Wi-Fi
- Bluetooth
- GPS - Satellite Navigation
- NFC - Near Field Communication
- Digital Radio
- WiGig
- Cellular Radio, including 2G/2.5G/3G/4G/5G
- WWAN - Wireless WAN
- SSD - Solid-State Drive

2.1.1 Form Factor

M.2 modules are rectangular and have an edge connector, with gold plated fingers, on one side. Multiple module sizes are defined/supported by the standard. Width can be 12, 16, 22 or 30 mm and lengths can be 16, 26, 30, 38, 42, 60, 80 or 110 mm.

The M.2 module code contain both the width and length of the specific module, so for example, module code 2230 means that the module is 22 mm wide and 30 mm long. 2230 is a common form factor used for WiFi/BT modules. The longer modules are typically used for large capacity SSD disks.

The M.2 connector has 75 positions, but due to keying (see below), only up to 67 positions can be used at the same time (less if multiple keying schemes are supported). The connector pitch is 0.5mm.

The M.2 module code also contains information about top and bottom side maximum component height. To be save always allow for 1.5mm component height on both top and bottom side.

2.1.2 Keying

The M.2 connector has different keying notches (typically one, but can be two) that demotes the supported hardware interfaces and the purpose of the connected M.2 module. There are different key identifications, represented by a single letter, A to M.

Embedded Artists' Wi-Fi/Bluetooth M.2 modules have key id; E, which defines pinning for PCIe (2x), SDIO, UART, PCM, USB2.0 and I2C interfaces.

Some key definitions overlap, for example A, B, E and M all supports at least one PCIe interface and B and M supports a SATA interface. An M.2 module can support two keying schemes at the same time and consequently have two key notches in the edge connector.

For more information about the M.2 standard, see: <https://en.wikipedia.org/wiki/M.2>

The official M.2 specification (PCI Express M.2 Specification) is available via membership from: www.pcisig.com

2.2 Non-standard M.2 Modules

Embedded Artists has added a non-standard feature on some of the 2230 M.2 modules designed together with Murata and Cypress. The pictures below illustrates how the standard module size has been extended by 14mm in the length direction in order to include a PCB trace antenna.

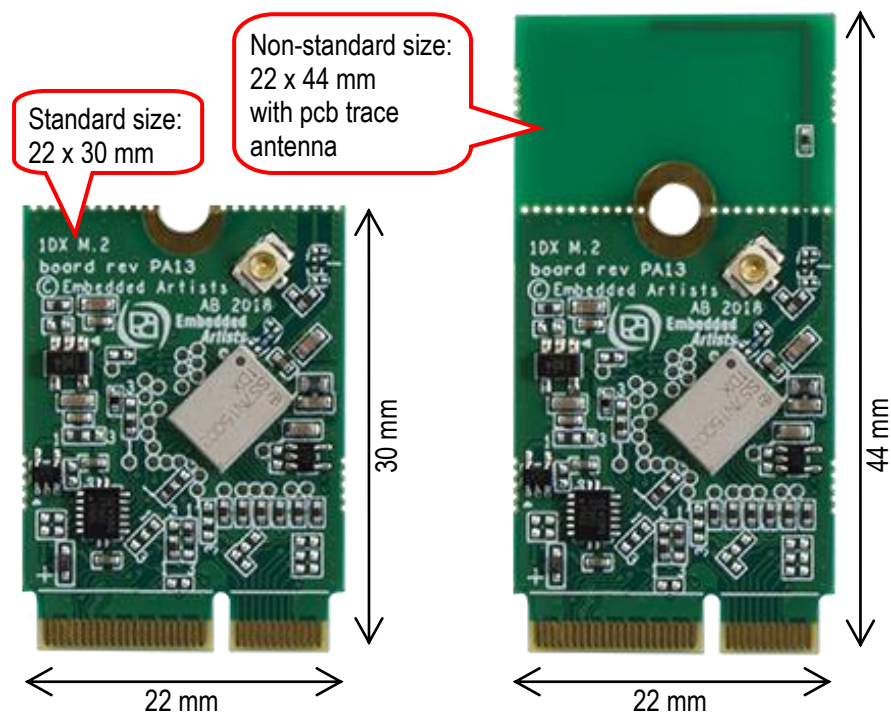


Figure 1 – M.2 Module With, and Without, Trace Antenna

The middle hole (or half hole) is the ground reference. It is important to ground this (half) hole with an M.2 screw with a larger head than normal M2 screws. Note that grounding is important even though the on-board PCB trace antenna is not used (or does not exist).

See the respective M.2 module datasheet for detailed information about clearance distances around the antenna.

M.2 modules with a pcb trace antenna has the antenna connected per default. It is possible to break-off the trace antenna to get a standard-sized M.2 module and then do a small rework to connect the antenna signal to the u.fl. antenna connector. See the respective M.2 module datasheet for detailed information about this rework.

2.3 Why Use M.2 Modules?

The obvious question is; Why use an M.2 module to add Wi-Fi/BT connectivity to a design?

Let's take a step back and look at the two main options available:

- **Wi-Fi/Bluetooth module**

A module integrates Wi-Fi/BT chipset, antenna PA, antenna switch, balun, crystal, passives and part of the power supply solution. A module is most often shielded, either with a metal can or a shielded resin is used to build the module. The pros and cons are listed below:

- + On components in the BOM to order instead of many (50+)
- + Can buy modules in small volume
- + Requires less RF and general design competence to integrate
- + Value-added module suppliers support the SW drivers for the module/chipset
- + Modules can be reference certified, allowing easier/lower-cost regulatory certification for customers
- Higher cost than chipsets

- **Wi-Fi/Bluetooth chipset**

A chipset can be integrated directly into the PCB of the design. The pros and cons are listed below:

- + Lowest cost if the volume is high
- + Most flexible solution
- Requires more RF and design competence. Requires some kind of shielding.
- Must make sure the chipset manufacturer will give SW support (which they will only do to very high volume customers).
- You cannot buy the chipsets directly unless you have very high volumes (100K+ pcs/year).
- Very small pitch BGA packages that requires expensive PCB process. This is not a solution for large area PCBs because the whole PCB will be expensive.
- Test and certification cost is very high.

Given above, for volume below 100K pcs/year, **the only real option is to use a Wi-Fi/BT module. Embedded Artists use Wi-Fi/BT modules from Murata to build M.2 modules**, which is a value-added module suppliers that provide excellent SW driver support.

To sum up and return to the question asked in the beginning of this section (*Why use an M.2 module to add Wi-Fi/BT connectivity to a design?*), there are multiple advantages of using M.2 modules in an embedded design, especially for lower volume design in the 1-20K pcs / year region.

- It is a modular and flexible approach to evaluate different Wi-Fi/BT solutions - with different trade-offs like performance, power consumption, range, cost, temperature range, supported standards, longevity, etc.
- It is a ready-to-go solution with minimal design work. No RF expertise is required - use the reference certified antenna or add external antenna
- Much more flexible solution than a direct solder down solution (that would require a redesign, and recertification if the module must be changed) -
- Supported by Embedded Artists' Developer's Kits for i.MX RT/6/7/8 development, including advanced debugging support on carrier boards. It also gives access to maintained software drivers (Linux and WICED) with responsive support from Murata.

Last, but not least, Embedded Artists' M.2 modules have been developed in close cooperation with Murata and Cypress. This ensures excellent and professional support!

3 M.2 Pinning

This chapter presents the pinning used for the M.2 modules from Embedded Artists. It is essentially M.2 Key-E compliant with enhancements to support additional debug signals and 3.3V VDDIO override. The pin assignment for specific control and debug signals has been jointly defined by Embedded Artists, Murata and Cypress.

The Wi-Fi interface is either SDIO or PCIe, depending on the used Murata module.

The Bluetooth interface is UART (and PCM for audio) or USB, depending on the used Murata module.

Optionally, an NFC interface can also be supported via I2C, USB or UART

Note that this information in the table below is not a complete copy of the M.2 specification. For specific details see the official M.2 specification (PCI Express M.2 Specification), which is available via membership from: www.pcisig.com

The picture below illustrates the edge pin numbering. It starts on the right edge and alternates between top and bottom side. The removed pads in the keying notch counts (but as obviously non-existing).

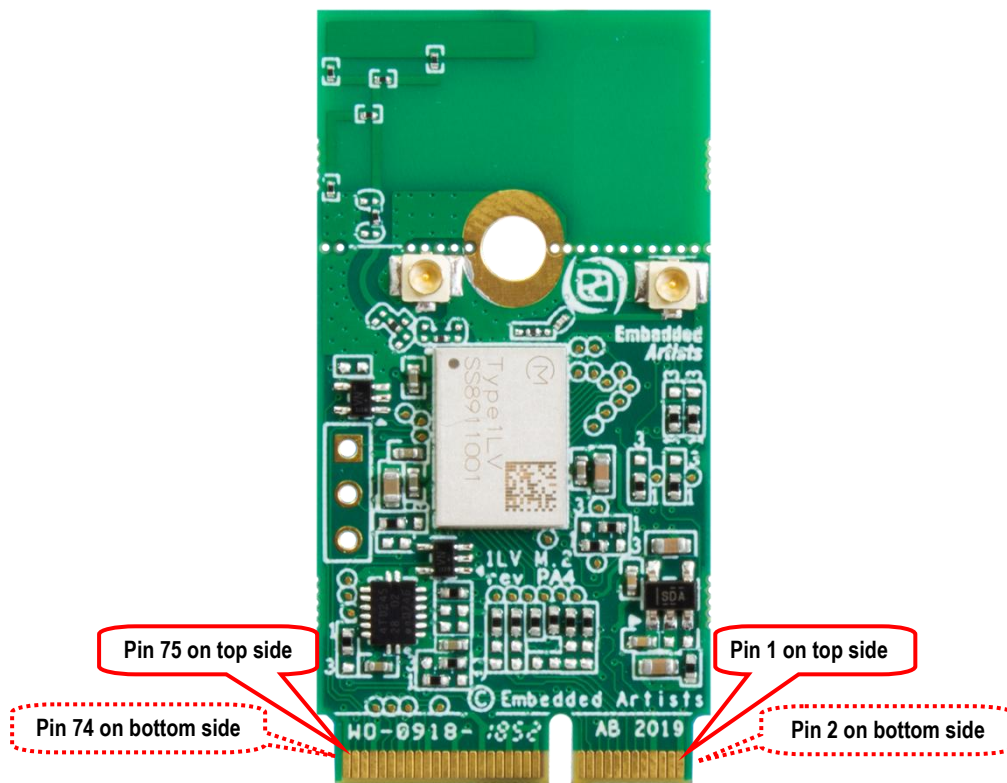


Figure 2 – M.2 Module Pin Numbering

The Wi-Fi interface uses either the SDIO or the PCIe interface. The Bluetooth interface uses the UART interface for control and PCM interface for audio. The column "When is signal needed" signals six different categories:

- Always: These signals shall always be connected.
- Wi-Fi SDIO: These signals shall always be connected then the Wi-Fi SDIO interface is used.
- Wi-Fi PCIe: These signals shall always be connected then the Wi-Fi PCIe interface is used.
- Bluetooth: These signals shall always be connected then the Bluetooth interface is used.

- Bluetooth audio: These signals shall always be connected then the Bluetooth audio interface is used.
- Optional: These signals are optional to connect, e.g., debug interfaces.

The table below lists the pin usage for a general M.2 module with E keying and SDIO or PCIe interface. Note that all M.2 modules do not support all pins and features. See the specific M.2 module datasheet for details.

Note that the M.2 standard defines different voltage levels on different pins. Both 1.8V and 3.3V signaling is used.

Pin #	Side of pcb	M.2 Name	Voltage Level and Signal Direction	When is signal needed	Note
1	Top	GND	GND	Always	Connect to ground
2	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply. Current consumption depends on used M.2 module. Up to 3A might be needed for some mimo Wi-Fi modules.
3	Top	USB_D+	-		Currently not used, but can be in the future.
4	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply. Current consumption depends on used M.2 module. Up to 3A might be needed for some mimo Wi-Fi modules.
5	Top	USB_D-			Currently not used, but can be in the future.
6	Bottom	LED_1#	OD output from M.2		Currently not used, but can be in the future.
7	Top	GND	GND	Always	Connect to ground
8	Bottom	PCM_CLK	1.8V I/O	Bluetooth audio	For Bluetooth audio interface: BT_PCM_CLK
9	Top	SDIO CLK	1.8V Input to M.2	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_CLK
10	Bottom	PCM_SYNC	1.8V I/O	Bluetooth audio	For Bluetooth audio interface: BT_PCM_SYNC
11	Top	SDIO CMD	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_CMD Note: Require an external 10-50K ohm pullup
12	Bottom	PCM_OUT	1.8V output from M.2	Bluetooth audio	For Bluetooth audio interface: BT_PCM_OUT
13	Top	SDIO DATA0	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D0 Note: Require an external 10-50K ohm pullup
14	Bottom	PCM_IN	1.8V input to M.2	Bluetooth audio	For Bluetooth audio interface: BT_PCM_IN
15	Top	SDIO DATA1	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D1 Note: Require an external 10-50K ohm pullup
16	Bottom	LED_2#	OD output from M.2		Currently not used, but can be in the future.
17	Top	SDIO DATA2	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D2 Note: Require an external 10-50K ohm pullup
18	Bottom	GND		Always	Connect to ground
19	Top	SDIO DATA3	1.8V I/O	Wi-Fi SDIO	For Wi-Fi SDIO interface: SDIO_D3 Note: Require an external 10-50K ohm pullup
20	Bottom	UART WAKE#	3.3V OD output from M.2	Bluetooth	For Bluetooth UART interface: BT_HOST_WAKE_L Require an external 10K pullup resistor to 3.3V.
21	Top	SDIO WAKE#	1.8V OD output from M.2	Wi-Fi SDIO	For Wi-Fi SDIO interface: WL_HOST_WAKE_L Require an external 10K pullup resistor to 1.8V.
22	Bottom	UART TXD	1.8V output from M.2	Bluetooth	For Bluetooth UART interface: BT_UART_TXD
23	Top	SDIO RESET#	1.8V input to M.2		Not used

24	Key, non existing				
25	Key, non existing				
26	Key, non existing				
27	Key, non existing				
28	Key, non existing				
29	Key, non existing				
30	Key, non existing				
31	Key, non existing				
32	Bottom	UART_RXD	1.8V input to M.2	Bluetooth	For Bluetooth UART interface: BT_UART_RXD
33	Top	GND		Always	Connect to ground
34	Bottom	UART_RTS	1.8V output from M.2	Bluetooth	For Bluetooth UART interface: BT_UART_RTS
35	Top	PERp0	PCIe data input to M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: transmit data from host processor
36	Bottom	UART_CTS	1.8V input to M.2	Bluetooth	For Bluetooth UART interface: BT_UART_CTS
37	Top	PERn0	PCIe data input to M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: transmit data from host processor
38	Bottom	VENDOR DEFINED	1.8V I/O	Optional	GPIO5-JTAG_TDO
39	Top	GND		Always	Connect to ground
40	Bottom	VENDOR DEFINED	1.8V I/O	Optional	GPIO4-JTAG_TDI
41	Top	PETp0	PCIe data output from M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: receive data to host processor
42	Bottom	VENDOR DEFINED	1.8V input to M.2	Bluetooth	BT_DEV_WAKE_L
43	Top	PETn0	PCIe data output from M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: receive data to host processor
44	Bottom	COEX3	1.8V I/O	Optional	GPIO6-JTAG_TRST
45	Top	GND		Always	Connect to ground
46	Bottom	COEX_TXD	1.8V I/O	Optional	GPIO2-JTAG_TCK
47	Top	REFCLKp0	PCIe clock input to M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: 100MHz reference clock input
48	Bottom	COEX_RXD	1.8V I/O	Optional	GPIO3-JTAG_TMS
49	Top	REFCLKn0	PCIe clock input to M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: 100MHz reference clock input
50	Bottom	SUSCLK	3.3V input to M.2	Always	External sleep clock input (32.768kHz)
51	Top	GND		Always	Connect to ground
52	Bottom	PERST0#	3.3V input to M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: Reset input signal, active low.
53	Top	CLKREQ0#	3.3V OD output from M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: Clock request output from M.2 Require an external 10K pullup resistor to 3.3V.
54	Bottom	W_DISABLE2#	3.3V input to M.2	Bluetooth	BT_REG_ON, High = BT enabled, Low = BT disabled
55	Top	PEWAKE0#	3.3V input to M.2	Wi-Fi PCIe	For Wi-Fi PCIe interface: Wakeup request from M.2 Require an external 10K pullup resistor to 3.3V.
56	Bottom	W_DISABLE1#	3.3V input to M.2	Wi-Fi	WL_REG_ON, High = Wi-Fi enabled, Low = Wi-Fi disabled
57	Top	GND		Always	Connect to ground
58	Bottom	I2C_SDA	1.8V I/O		Currently not used, but can be in the future.
59	Top	Reserved	1.8V I/O	Optional	BT_GPIO2
60	Bottom	I2C_CLK	1.8V input to M.2		Currently not used, but can be in the future.

61	Top	Reserved	1.8V I/O	Optional	BT_GPIO3
62	Bottom	ALERT#	1.8V OD output from M.2	Optional	WL_GPIO11_RTS_ALERT Require an external 10K pullup resistor to 1.8V.
63	Top	GND		Always	Connect to ground
64	Bottom	RESERVED			On some M.2 modules from Embedded Artists it is possible to apply a 3.3V supply (100 mA) to this signal in order to get 3.3V voltage level on all signals.
65	Top	Reserved	1.8V output from M.2	Optional	BT_GPIO4_RTS
66	Bottom	UIM_SWP	1.8V I/O	Wi-Fi SDIO	WL_DEV_WAKE & GPIO1 & GPIO10_CTS
67	Top	Reserved	1.8V input to M.2	Optional	BT_GPIO5_CTS
68	Bottom	UIM_POWER_SNK	1.8V output from M.2	Optional	WL_GPIO9_TXD WL debug channel UART
69	Top	GND		Always	Connect to ground
70	Bottom	UIM_POWER_SRC/GPIO_1	1.8V input to M.2	Optional	WL_GPIO8_RXD WL debug channel UART
71	Top	Reserved	1.8V output from M.2	Optional	BT_GPIO6_TXD BT debug channel UART
72	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply. Current consumption depends on used M.2 module. Up to 3A might be needed for some mimo Wi-Fi modules.
73	Top	Reserved	1.8V input to M.2	Optional	BT_GPIO7_RXD BT debug channel UART
74	Bottom	3.3 V		Always	Power supply input. Connect to stable, low-noise 3.3V supply. Current consumption depends on used M.2 module. Up to 3A might be needed for some mimo Wi-Fi modules.
75	Top	GND		Always	Connect to ground

4 M.2 Integration Guide - On Carrier Board

This chapter presents how to design an M.2 interface and also contains a checklist. The integration process is outlined in a step-by-step process.

4.1 Step #1: Decide which interfaces to support

There are several interfaces that can be supported. All of them are not always needed. Which ones to support depends on if a general M.2 interface shall be created or just for a specific M.2 module. It also depends on if the optional debug interfaces shall be supported.

Interface	When to implement	Signals
Powering and enable controls	Always implemented	VBAT (3.3-3.6V) WL_REG_ON_3V3 BT_REG_ON_3V3 32.768KHZ_CLK_3V3
Wi-Fi SDIO	Implement if Wi-Fi has SDIO interface	6 SDIO signals (1.8V) WL_HOST_WAKE_1V8 WL_DEV_WAKE_1V8 BT_HOST_WAKE_3V3 BT_DEV_WAKE_1V8
Wi-Fi PCIe	Implement if Wi-Fi has PCIe interface	6 PCIe signals PCIE_CLKREQ_L_3V3 PCIE_PME_L_3V3 PCIE_PERST_L_3V3
BT UART	Implement if the Bluetooth interface shall be supported	4 UART signals, 1.8V
BT Audio	Implement if the audio interface of Bluetooth shall be supported	4 PCM signals, 1.8V
Debug	Implement selected parts of debug interfaces if extra debug support is wanted. Note that all M.2 modules do not support all debug interfaces. Also note that the debug interfaces are not always openly documented. Support from Murata and/or Cypress is likely to be needed to utilize the features.	5 JTAG signals (1.8V) 2-4 BT debug UART (1.8V) 2-4 WL debug UART (1.8V)

4.2 Step #2: Decide SDIO and interface voltage

The M.2 standard defines two voltage levels that are used, 1.8V (for most data patch signals) and 3.3V (for some control signals).

If compatibility and overall support for most M.2 modules is important, then follow the standard. Voltage level shifters will be needed in the design.

If the interface is designed for a specific M.2 modules, then there is a feature on some (not all) M.2 modules from Embedded Artists to change the voltage level of the 1.8V signals to 3.3V for all. Supply a 3.3V voltage to pin 64 on the M.2 connector. Verify with the M.2 module datasheet if this 1.8V VDDIO override is supported, or not. The table below lists the M.2 modules available as of May 2019.

M.2 Module	Support for alternative voltage levels
1DX M.2	Supports 3.3V VDDIO override on 1.8V signals.
1MX M.2	Supports 3.3V VDDIO override on 1.8V signals, but requires a small modification/rework on the M.2 PCB if SDIO voltage level shall be 3.3V
1LV M.2	Do NOT support 3.3V VDDIO override on 1.8V signals and SDIO voltage level is fixed at 1.8V.
1CX M.2	Supports 3.3V VDDIO override on 1.8V signals.

Note that SDIO voltage level is 1.8V, as specified in the M.2 standard. It is not allowed to start at 3.3V and then switch to 1.8V signaling (as is normally done for an SD card interface). The signaling voltage level should be fixed at 1.8V.

When 3.3V VDDIO override on 1.8V signals is used, the SDIO voltage level is 3.3V.

4.3 Step #3: Decide VBAT voltage and current

Design the VBAT power supply after maximum current consumption, see the Murata module datasheet for details. Add sufficient margin, at least 30%.

Select the VBAT voltage - 3.3V is the normal value, but this is often the lower value for the module's RF specification. Having a power supply with +/-10% accuracy can result in operating the module outside of specification. Either design the power supply with tight absolute voltage tolerance or increase to for example 3.6V. Note that 3.6V is maximum voltage even though the Murata modules accept higher VBAT voltage, but other components on the M.2 module limits the maximum voltage to 3.6V.

Make sure the design is low-noise because the RF performance can be severely negatively affected if there is too much noise on the VBAT supply voltage. A linear power supply design is preferred over switched dc/dc converted, but is not always possible to efficiency reasons. Pay attention to transient response on the power supply since current bursts can be short for example during transmit.

Note that VBAT shall not rise (10 - 90%) faster than 40 microseconds and not slower than 100 milliseconds.

4.4 Step #4: Select M.2 connector and stand-off

Embedded Artists use the MDT420E03001 connector from Amphenol, (Digikey part number: MDT420E03001CT-ND). The connector gives 2.54 mm clearance between the bottom side of the mounted M.2 module and the PCB (that the connector is mounted on). There are M.2 connectors with both more and less clearance. If another connector is selected, make sure it is E-key and that the clearance under the mounted M.2 module is sufficient. If no components are mounted under the area that the M.2 module occupy, the clearance can be minimal. Check the M.2 module datasheet for details about bottom side components. For a general design that shall be able to accept all types of M.2 modules (that follow the M.2 standard), make the clearance at least 1.5 mm.

Select a proper standoff for the grounding point in the middle of the M.2 module. The stand-off material shall be metal since it shall be conducting to give a proper grounding point. Note that different M.2 connectors have different heights for the M.2 module over the base PCB. The stand-off must match this height. Embedded Artists use the SM3ZS067U410-NUT1-R1200 stand-off from JAE (Digikey part number: 670-2865-1-ND) and this match the MDT420E03001 connector (2.45mm high)

4.5 Step #5: Create schematic and verify checklist

Create the schematic. Embedded Artists has published schematics for two carrier boards that implement the M.2 interface. These schematics can be used as reference when creating the schematic for your specific design. These schematics are part of the M.2 Primer zip-file.

- *iMX Developer's Kits*, where the carrier board is named *COM Carrier Board, rev E* (and above). This design support both Wi-Fi SDIO and PCIe interfaces, has variable 3.3V/3.6V VBAT, variable 1.8/3.3V VDDIO override and implements all debug interfaces.
- *iMX RT1062 Developer's Kit*, where the carrier board is named *iMX OEM Carrier Board, rev B* (and above). This design support Wi-Fi SDIO interface, has an optional 3.3V/3.6V VBAT, 1.8V SDIO voltage, no VDDIO override and implements all debug interfaces.
- There are also two schematics that show the core designs for SDIO and PCIe.

Use the following checklist to verify that the design is correct. Note that this checklist is not exhaustive and there is no guarantee that the design will work just by following the list, but it will increase the likelihood for success.

Schematic checklist:

- Verify that the voltage levels for all signals is correct (1.8V or 3.3V).
- If 3.3V VDDIO override on 1.8V signals is used, verify that the M.2 module supports it.
- Verify that VBAT do not rise (10 - 90%) faster than 40 microseconds and not slower than 100 milliseconds.
- Verify that signals WL_REG_ON or BT_REG_ON have correct timing. They must be held low for at least 700 microseconds after supply voltage has reached specification level before pulled high. 2 clock cycles of the 32.678kHz clock must also have passed before any of the signals is pulled high. These clock cycles will typically occur during the 700 microseconds but if the clock signal has a long delay during power-up, the 700 microsecond period can be extended
- Verify that the 32.768 kHz clock has 3.3V signaling and a frequency accuracy of +-200 ppm, or better. Verify with M.2 datasheet for details.
- Add two 100 nF X7R/X5R ceramic capacitors and two 22uF X7R/X5R ceramic capacitors on VBAT. Voltage rating on the capacitors should be at least 10V.
- If SDIO interface:

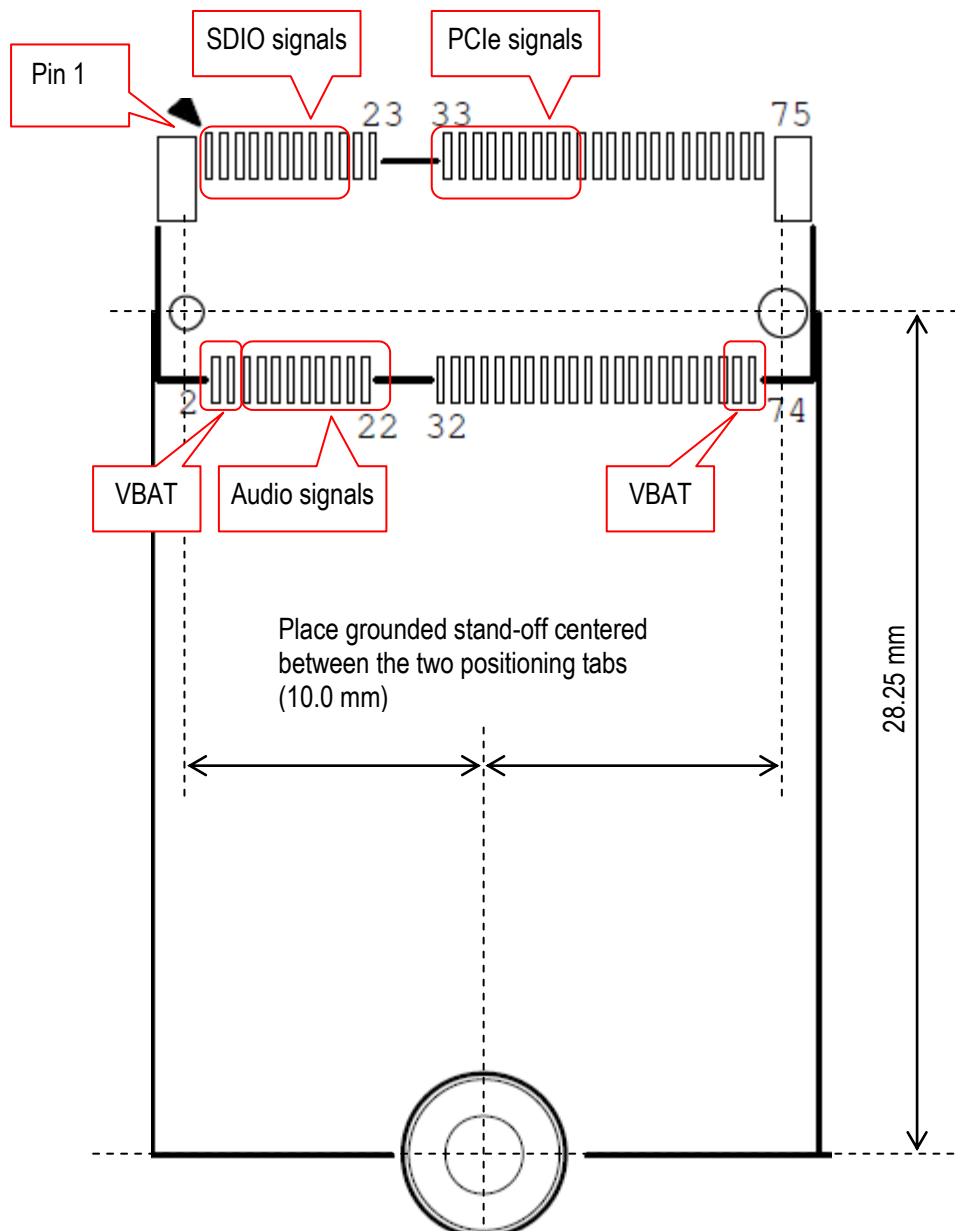
- Verify that SDIO voltage is fixed at 1.8V (or 3.3V, if 3.3V VDDIO override is used). This is important also during startup/boot of the system.
 - Verify that SDIO_CMD, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, SDIO_DATA3 all have 10-50K pullups.
 - Verify that there is a 10K pullup to 1.8V on signal SDIO_WAKE#.
- If PCIe interface:
 - Verify that there is a 10K pullup to 3.3V on signal PEWAKE0#, 10K pullup to 3.3V on signal CLKREQ0# and 10K pullup to 3.3V on signal PERST0#.
 - Verify that there are 50 ohm parallel termination resistors on the PCIe_CLK signal pair.
 - Verify that direction on receive and transmit data pairs is correct.
- If BT interface:
 - Verify that there is a 10K pullup to 3.3V on signal UART_WAKE#.
 - Verify that the direction of RTS/CTS signals are correct. As a failsafe, it can be good idea to add an switch the signals.
 - Verify the directions of the UART signals (RXD connects to TXD and vice versa).
- If BT audio interface:
 - Verify that the direction of the audio interface signals is correct.

4.6 Step#6: Create layout and verify checklist

Create the layout of the schematic. Use the following checklist to verify that the layout is correct. Note that this checklist is not exhaustive and there is no guarantee that the design will work just by following the list, but it will increase the likelihood for success.

Layout checklist:

- Verify that pin numbering on the M.2 connector is correct, see picture below. A couple of signal groups are marked in the picture and can be used to verify correct pin numbering and orientation of the M.2 connector.



- If SDIO interface:
 - Verify that SDIO signals are routed with correct impedance (50 ohm) over a solid reference plane (GND preferred, but not strictly needed).
 - Verify that the 6 SDIO signals are length matched to 100 mil (if SDIO_CLK is up to 50MHz) or 25 mil (if SDIO_CLK is up to 200MHz).

- If PCIe interface:
 - Verify that PCIe signals are routed with correct impedance over a solid reference plane (GND preferred, but not strictly needed). PCIe data pairs shall have 85 ohm differential impedance and PCIe clock pair shall have 100 ohm differential impedance.
 - Verify that PCIe signals follow general PCIe routing guidelines.
 - Verify that the two 50 ohm parallel termination resistors on the PCIe_CLK signal pair are placed close to the M.2 connector.
- Verify that the grounded stand-off is placed at correct location, see picture above.
- Verify that clearance under the M.2 module area is enough. Unless absolutely needed, avoid placing components under the area the M.2 module is mounted.
- If using the on-board PCB trace antenna in the final product, verify that clearance distances are observed. Ideally, arrange the M.2 module so that the antenna is located at a corner of the product. Keep plastic case (i.e., non-metallic) away from the antenna area with at least 5 mm clearance (in all directions). Note that this is a general recommendation - see the specific M.2 module datasheet for details. Also keep any metal elements (e.g., connectors, battery, etc.) away from the antenna area with at least 5 mm clearance (in all directions). Keep a clearance area under and above the antenna area of at least 7.5mm, both under and over the PCB. Human hands or body parts should be kept away (in the normal use case) from the antenna area.

4.7 Step #7: Verify signal and power quality

Verify the signal and power quality on the prototypes. This section will demonstrate how the SDIO interface can be verified and also optimized. The i.MX processors can configure different drive strength on the SDIO interface (and all I/O signals in general). The effect of that is also presented.

First of all, measuring high speed signals is a challenge. The picture below illustrates SDIO_CLK with a 50MHz clock measures with an active probe having 1.0pF capacitance and 1 GHz bandwidth. The bandwidth of the oscilloscope is 500 MHz.

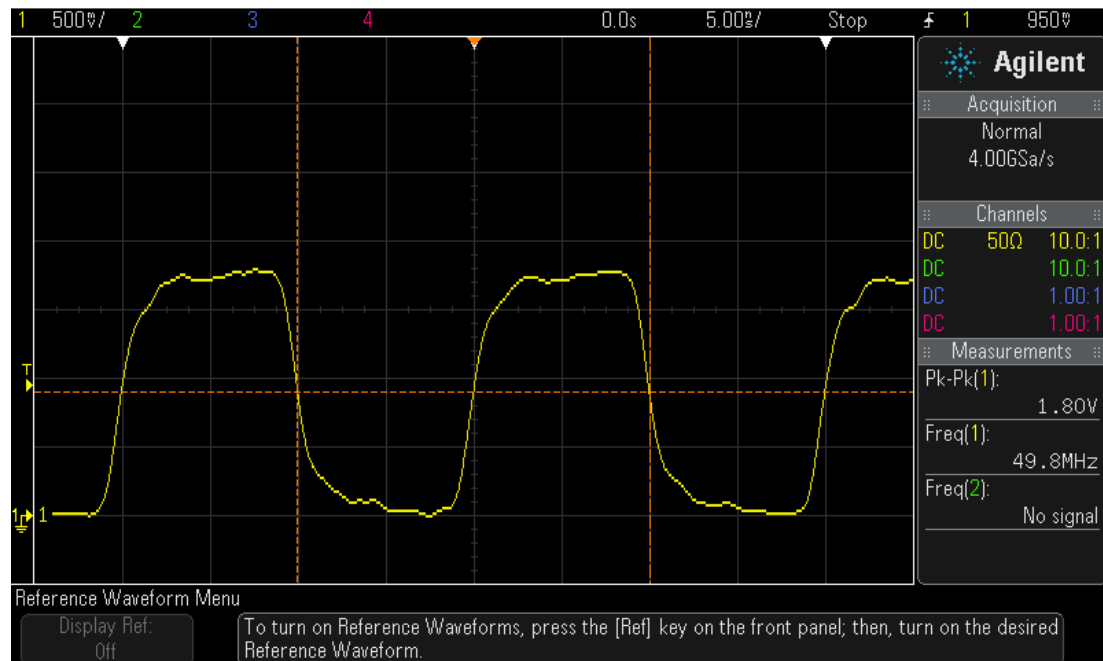


Figure 3 – 50 MHz SDIO_CLK measured with active probe

The picture below illustrates the same SDIO_CLK measures with a passive probe having 11pF capacitance and 500 MHz bandwidth. The signal measured with the active probe is placed in the background as a reference. The signals are relatively similar, but not identical.

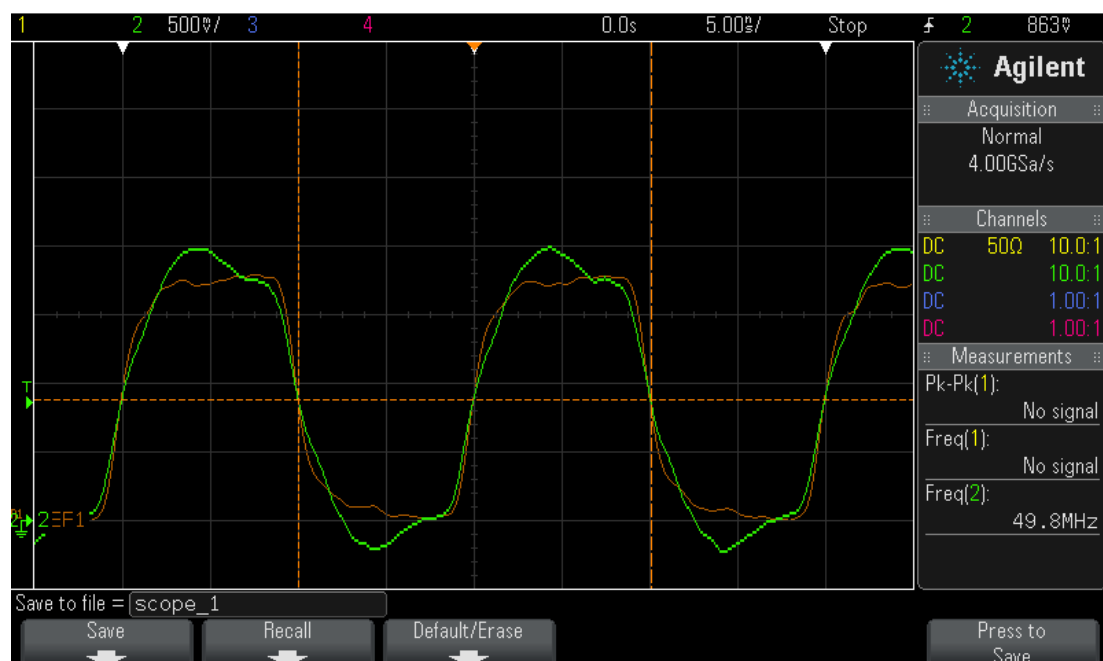


Figure 4 – 50 MHz SDIO_CLK measured with passive probe (active probe measurement in reference background)

Below is a 200 MHz SDIO_CLK signals. The orange trace is when measuring with an active probe and the green trace with a passive probe. Here the signals are clearly different and illustrates the importance of measuring high speed signals with a low capacitance probe in order to affect the signal as little as possible.

Also note that the bandwidth of the oscilloscope is 500 MHz, which is too low for measuring a 200 MHz signals with any accuracy. This is also something to consider.

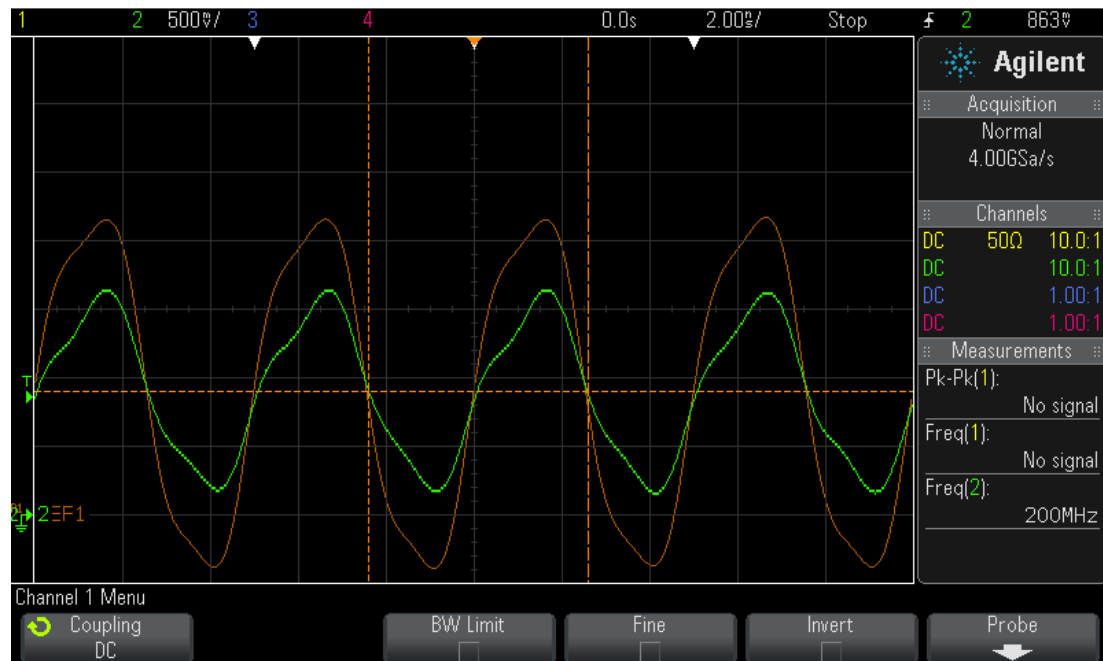


Figure 5 – 200 MHz SDIO_CLK measured with passive probe (active probe measurement in reference background)

The following measurements have been done with an active probe. The picture below illustrates how signal drive strength affect the signal quality. The orange reference trace is the 50 MHz SDIO_CLK seen in the first picture in this section. Drive strength is 75 ohm, medium speed. The yellow trace is when the drive strength is set to 255 ohm, medium speed. Clearly much too low drive strength.

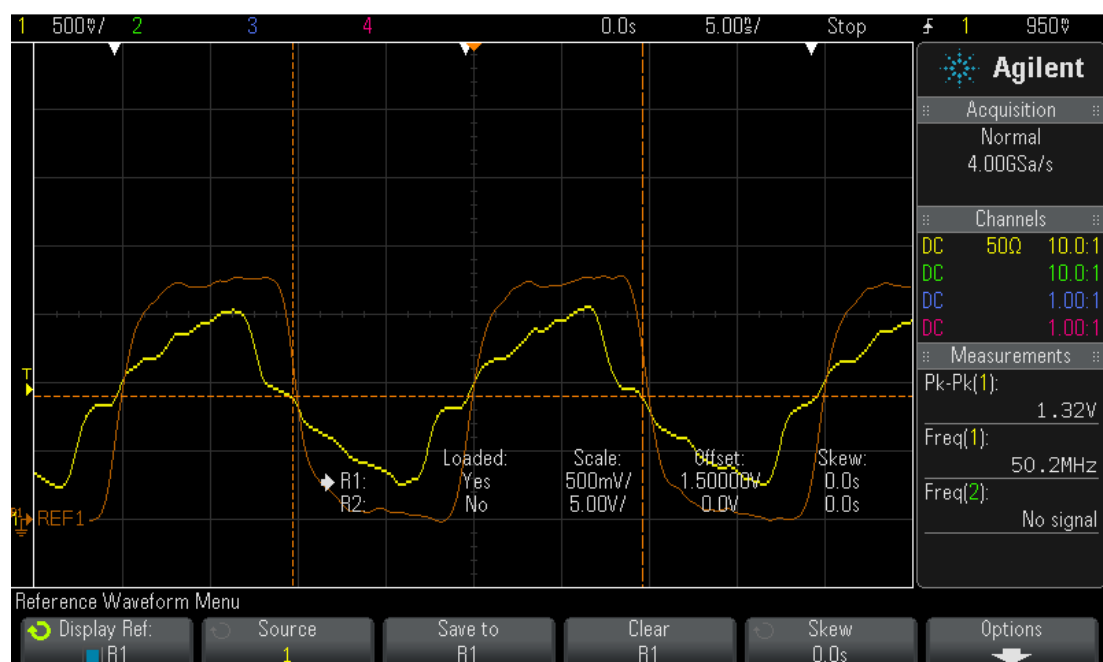


Figure 6 – 50 MHz SDIO_CLK with optimized and low drive strength

The picture below illustrates how it is possible to trim the drive strength, often in small steps. The orange reference trace is the same as before, a 50MHz SDIO_CLK with 75 ohm, medium speed drive strength. The yellow trace is when the drive strength is set to 105 ohm, medium speed. As seen, 75 ohm is clearly better and there is no over/undershoots.

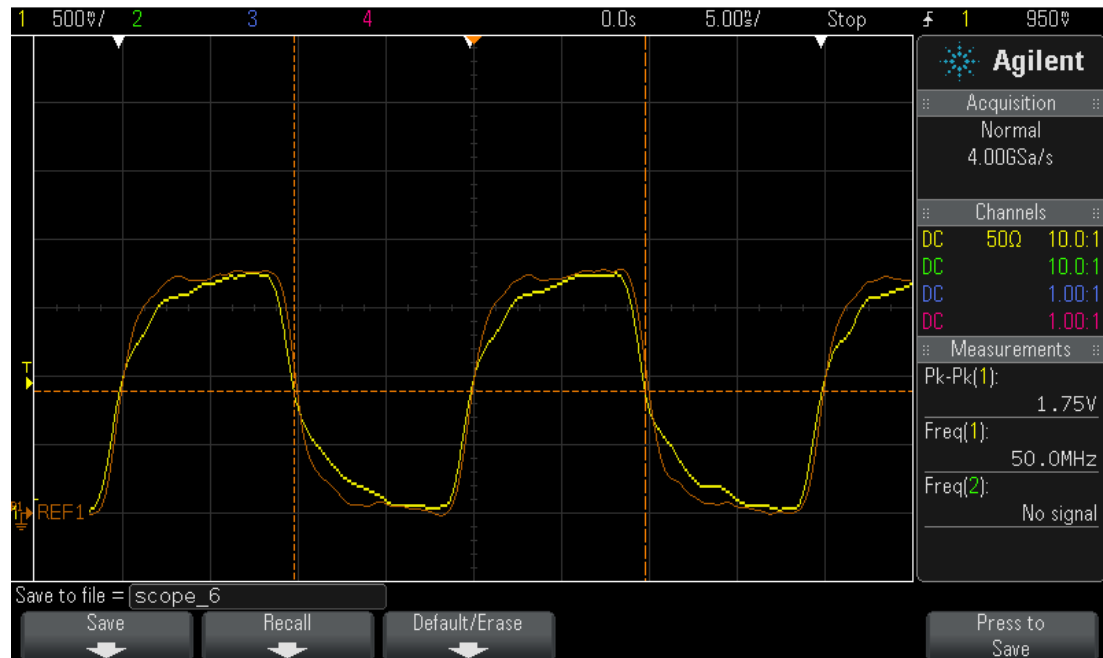


Figure 7 – 50 MHz SDIO_CLK with optimized and slightly low drive strength

The final picture illustrates when the drive strength is too high. The reference trace is the same as before, a 50MHz SDIO_CLK with 75 ohm, medium speed drive strength. The yellow trace is when the drive strength is set to 40 ohm, max speed. There are clear over/under shoots on the signal which affect the RF performance of the module.

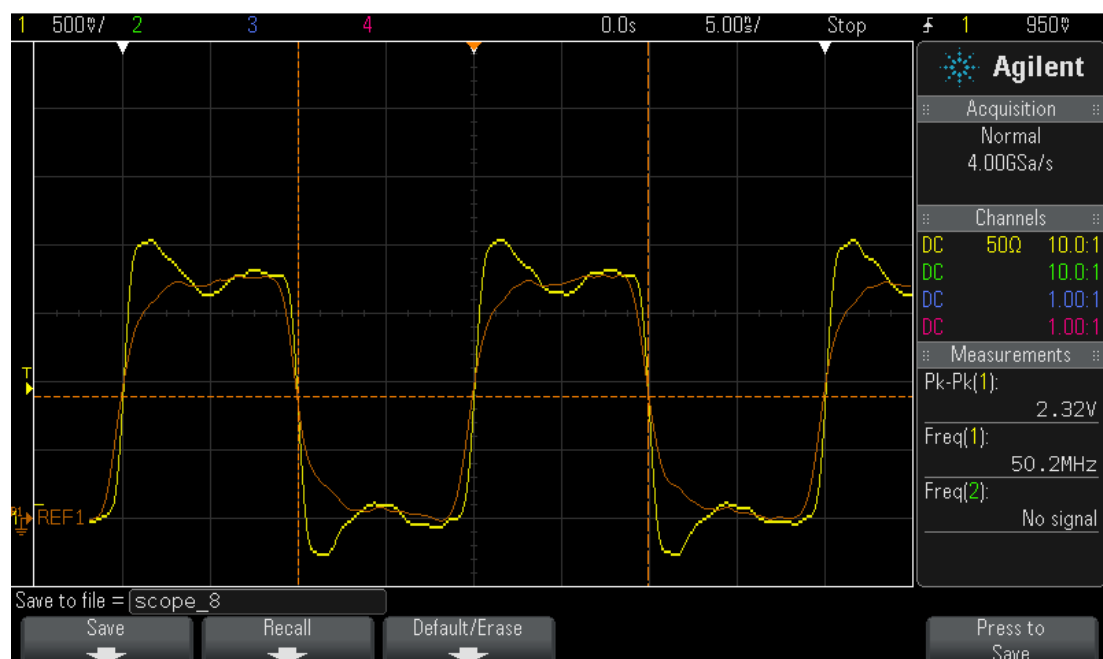


Figure 8 – 50 MHz SDIO_CLK with optimized and too high drive strength

See the M.2 module datasheet for details where to measure the SDIO signals. The signal quality should be verified as close to the Murata module as possible, so the test pads on the M.2 module shall be used. It is not correct to measure for example on the M.2 connector or at the i.MX processor side.

Adjust the SDIO bus drive strength so that signals have clean, defined edges and no over/under shoots. Verify that selected settings give reliable performance over the product's temperature range. There is no need to try to create a perfect looking square wave (for the SDIO_CLK signal) because that will general unnecessary EMC emission.

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